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PATENT APPLICATION

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CASE 12-14-9-7-5

TITLE A Method Of Fabricating A Heterojunction Bipolar Transistor

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SIR:

NEW APPLICATION UNDER 37 CFR 1.53(b)

Enclosed are the following papers relating to the above-named application for patent:

Specification  
3 Formal sheets of drawing(s)  
1 Assignment with Cover Sheet  
Declaration and Power of Attorney  
Information Disclosure Statement

CLAIMS AS FILED				
	NO. FILED	NO. EXTRA	RATE	CALCULATIONS
Total Claims	20 - 20 =	0	x \$18 =	\$0
Independent Claims	3 - 3 =	0	x \$78 =	\$0
Multiple Dependent Claim(s), if applicable			\$260 =	\$0
Basic Fee				\$760
TOTAL FEE:				\$760

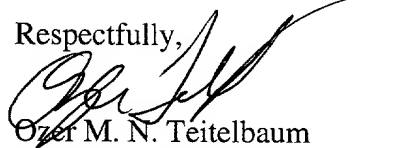
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# A METHOD OF FABRICATING A HETEROJUNCTION BIPOLAR TRANSISTOR

## 5 FIELD OF THE INVENTION

The present invention relates to semiconductors, generally, and more particularly to a method of fabricating a heterostructure device, such as a Double Heterojunction Bipolar Transistor ("DHBT").

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## BACKGROUND OF THE INVENTION

III-V bipolar transistors are three terminal devices having three regions of alternating conductivity type, referred to as the emitter, base, and collector, constructed from III and V semiconductor compounds. One class of III-V bipolar transistors gaining notoriety is heterostructure devices - heterojunction bipolar transistors ("HBTs") and double heterojunction bipolar transistors ("DHBTs"). HBT and DHBTs include a junction between materials of differing composition, such as InGaAs and InP. In such an exemplary device structure, the InGaAs material has several known distinct properties from the InP material. These characteristics are detailed in depth in various references, including Sze, Physics of Semiconductor Device, Wiley-Interscience, 1969, pp. 17-24 and 140-146 (hereinafter "Sze"), Williams, Gallium Arsenide Processing Techniques, Artech House, Inc., 1984, pp. 17-35 and 79-82 (hereinafter "Williams"), and Streetman, Solid State Electronic Devices, Prentice-Hall, Inc., 1980, pp. 52-96, 395-399, and 424-428 (hereinafter "Streetman") which are hereby incorporated by reference.

Various methods of fabricating III-V DHBT devices are known in the art. Referring to FIG. 1, a multi-layer structure 5 is shown prior to undergoing the

process steps for making a III-V DHBT device, as detailed in U.S. Patent Number 5,907,165, commonly assigned with the present invention and hereby incorporated by reference. Structure 5 is grown using standard growth techniques as known in the art, such as Metal-Organic Molecular Beam Epitaxy (MO-MBE). Structure 5 comprises an InP substrate layer 10 on which a series of semiconductor layers 20 through 80 are sequentially grown. A subcollector layer 20 is formed overlying InP substrate layer 10 and comprises n<sup>+</sup> doped InGaAs. Subcollector layer 20 also includes buffer layers to prevent unacceptable diffusion of impurities within the multilayer structure. The buffer layers comprise an n-doped InGaAs layer and an undoped InGaAs layer. An n- doped InP collector layer 30 is formed overlying subcollector layer 20.

III-V DHBTs are typically formed with buried junctions covered by thin graded quaternary layers to improve device reliability. Structure 5 of FIG. 1 comprises a base-collector and a base-emitter graded quaternary InGaAsP layer, 40 and 60, respectively. Collector-base graded quaternary layer 40 separates collector layer 30 from a base layer 50. Base layer 50 comprises a doped InGaAs. Collector-base graded quaternary layer 40 comprises a series of InGaAsP sublayers, including several buffer layers. These buffer layers are intended to improve transport characteristics and reduce current blocking, and comprise at least an n-doped InGaAs layer and an undoped InGaAs layer. Similarly, the emitter-base quaternary graded layer 60 comprises a series of InGaAsP sublayers for separating n-doped InP emitter layer 70 from base layer 50. Overlying emitter layer 70 is an n-type doped InGaAs emitter contact layer 80.

Referring to FIG. 2, a first series of steps are executed on the structure 5 of the known process is shown. Here, an emitter contact pad 90 is selectively formed overlying emitter contact layer 80 by a lift-off process, as is known in the art. A general description of the lift-off technique and its use may be found in

U.S. Patent Numbers 4,214,966, 5,620,909, 5,625,206, 5,656,515, and 5,903,037 each commonly assigned with the present invention, as well as Williams, pp.125-127, all of which are incorporated herein by reference. Emitter contact 90 has a lateral dimension of approximately  $3 \times 5 \mu\text{m}$ .

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As illustrated, emitter contact layer 80 is also wet or plasma etched using emitter contact pad 90 as an etch mask. An over-etch is performed to obtain an undercut as depicted under emitter contact pad 90 of  $0.1 \mu\text{m}$  or more. Patterned contact layer 80 then serves as the etch mask for emitter layer 70 in a subsequent wet etch step. Subsequently, a base contact 100 is formed by evaporating a base contact metal using emitter contact pad 90 as a shadow mask to define the inner edge of base contact 100.

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Subsequently, a base mesa is defined by a photolithographic resist step. The base mesa is thereafter selectively dry etched using  $\text{BCl}_3/\text{N}_2$ , thereby removing more than half the thickness of collector layer 30. The residual of collector layer 30 is then selectively wet etched and over-etched to produce an undercut. This undercut serves to reduce the base-collector capacitance of the III-V device. Thereafter, a collector contact 120 is deposited overlying the subcollector layer 20.

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Referring to FIG. 3, a final series of steps are executed on the structure of FIG. 2 to create the known DHBT. First, the structure of FIG. 2 is passivated and encapsulated with a common layer 130, such as a polymer encapsulant. The device structure is then selectively dry etched to form via holes 140 through encapsulant layer 130. In so doing, access is gained to the collector, base and emitter metallization contacts, respectively, such that conductive plugs 150 are evaporated thereafter into via holes 140 to complete the device.

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In the constant attempt to fabricate smaller III-V devices, it appears that the known art is limited to certain applications where the ability to finely dry etch via holes is not critical. Dry etching vias has proven effective for fabricating DHBTs having an emitter dimensions in the range of at least  $2 \times 4 \mu\text{m}$  to  $3 \times 5 \mu\text{m}$ . However, while the above known process for fabricating a III-V DHBT may provide for smaller device construction, dry etching vias for a transistor having an emitter of less than  $2 \times 4 \mu\text{m}$  has proven difficult. At these dimensions, the dry etched vias are difficult to define using lithography. This is particularly relevant with respect to the base and emitter vias because of the intended smaller device size. Presently, in view of the drive for smaller devices, a commercial interest exists for a DHBT device with an emitter contact dimension of at least  $1.2 \times 3 \mu\text{m}$ , as well as a base and emitter contact spacing of less than  $1 \mu\text{m}$ .

As a result, a method of manufacturing a DHBT is needed that will enable smaller device dimensions. Similarly, there is a demand for a process of fabricating a DHBT that is independent of dry etching vias to gain access to the base, emitter and collector contacts.

## SUMMARY OF THE INVENTION

To achieve the many advantages of the present invention, a method of fabricating a III-V semiconductor device is disclosed. The semiconductor device comprises areas within a device structure with defined mesas, as well as base, emitter and collector contact pads. The method comprises the steps of forming at least one collector contact post overlying at least one the collector contact pad and forming at least one base contact post overlying at least one the base contact pad. Subsequently, a passivation layer is formed over the device structure with defined mesas, base, emitter and collector contact pads. The passivation layer is

then cured. Thereafter, small segments of the encapsulating layer are exposed by performing an etch back step to fabricate a device and thereby reduce the dependence on via holes for gaining access to the base, emitter and collector contacts.

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These and other advantages and objects will become apparent to those skilled in the art from the following detailed description read in conjunction with the appended claims and the drawings attached hereto.

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### **BRIEF DESCRIPTION OF THE DRAWINGS**

The present invention will be better understood from reading the following description of non-limiting embodiments, with reference to the attached drawings, wherein below:

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**FIG. 1** is a cross-sectional view of a semiconductor substrate structure prior to undergoing steps of a known method;

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**FIG. 2** is a cross-sectional view of the semiconductor substrate structure of **FIG. 1** after undergoing a first series of steps according to the known method;

**FIG. 3** is a cross-sectional view of the semiconductor substrate structure of **FIG. 2** after undergoing a second series of steps to complete the device according to the known method;

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**FIG. 4** is a cross-sectional view of a semiconductor structure prior to undergoing a first step of the present invention;

FIG. 5 is a cross-sectional view of the semiconductor substrate structure of FIG. 4 after undergoing a first step of the present invention;

FIG. 6 is a cross-sectional view of a semiconductor substrate structure of FIG. 5 after undergoing a second step of the present invention;

FIG. 7 is a cross-sectional view of a semiconductor substrate structure of FIG. 6 after undergoing a third step of the present invention;

FIG. 8 is a top down view of a semiconductor substrate structure illustrated in FIG. 7; and

FIG. 9 is a graph illustrating the Frequency (GHz) versus  $I_c$  Current (A) characteristics of the resultant structure of the present invention.

It should be emphasized that the drawings of the instant application are not to scale but are merely schematic representations, and thus are not intended to portray the specific parameters or the structural details of the invention, which can be determined by one of skill in the art by examination of the information herein.

#### **DETAILED DESCRIPTION OF THE PRESENT INVENTION**

Referring to FIG. 4, a cross sectional view of a semiconductor structure 200 having defined mesas is illustrated prior to undergoing the steps of the present invention. Semiconductor structure 200 comprises an InP base substrate 210. Overlying InP layer 210 is a subcollector layer 220, also referred to as a collector contact layer. Subcollector layer 220 comprises n+ doped InGaAs and



has an advantageous thickness in the approximate range of 2500Å to 5000Å. Subcollector layer 220 is doped  $n^+$  with a dopant concentration of in the range of approximately  $2 \times 10^{19} \text{ cm}^{-3}$  to  $1 \times 10^{20} \text{ cm}^{-3}$ . It is advantageous to use Sn as the n-type dopant, although other n-type impurities such as Si may also be employed.

- 5 It is also beneficial for subcollector layer 220 to further comprise a series of buffer layers to prevent up-diffusion of impurities in the structure 200. These buffer layers comprise an n-doped InGaAs layer doped in the approximate range of  $1 \times 10^{18} \text{ cm}^{-3}$  to  $1 \times 10^{19} \text{ cm}^{-3}$  and having a thickness in the approximate range of 180Å to 220Å, as well as an undoped InGaAs layer having a thickness in the
- 10 approximate range of 18Å to 22Å.

- Formed overlying subcollector layer 220 is a collector layer 230. Collector layer 230 comprises InP. Collector layer 230 is n- doped with a concentration in the range of approximately  $1 \times 10^{16} \text{ cm}^{-3}$  to  $1 \times 10^{17} \text{ cm}^{-3}$ . Collector layer 230 has a
- 15 thickness in the approximate range of 2000Å to 5000Å.

- Further, semiconductor structure 200 comprises a base-collector graded quaternary InGaAsP layer 240 overlying collector layer 230. It is advantageous for base-collector graded quaternary layer 240 to comprises a InGaAsP
- 20 (approximately 1.13 eV) layer having a thickness approximately in the range of 115Å to 145Å and an InGaAsP (approximately 0.95 eV) layer having a thickness approximately in the range of 115Å to 145Å. Each InGaAsP layer is doped with a concentration level of in the range of approximately  $1 \times 10^{17} \text{ cm}^{-3}$  to  $1 \times 10^{18} \text{ cm}^{-3}$ . It may be also beneficial for layer 240, alternatively, to comprise a buffer layer. In
- 25 this alternate embodiment, the buffer layer advantageously comprises a graded InGaAsP layer that is n-doped approximately in the range of  $1 \times 10^{17} \text{ cm}^{-3}$  to  $1 \times 10^{18} \text{ cm}^{-3}$  and having a thickness in the approximate range of 270Å to 300Å, as well as an undoped InGaAs layer having a thickness in the approximate range of 180Å to 220Å.

Overlying base-collector graded quaternary InGaAsP layer 240 is a base layer 250. In an alternate embodiment, base layer 250 overlies the buffer layer. Base layer 250 comprises InGaAs. It is advantageous to dope InGaAs base layer 250 with carbon at a concentration in the approximate range of  $2 \times 10^{19} \text{ cm}^{-3}$  to  $1 \times 10^{20} \text{ cm}^{-3}$ . Moreover, it is beneficial for InGaAs base layer 250 to have a thickness in the range of approximately 200Å to 1000Å.

In one embodiment of the present invention, semiconductor structure 200 additionally comprises a base-emitter graded quaternary InGaAsP layer 260 overlying base layer 250. Here, emitter-base quaternary graded layer 260 comprises at least one InGaAsP (approximately 0.95eV) layer having a thickness in the range of approximately 65Å to 85Å. Alternatively, emitter-base quaternary graded layer 260 may comprise an InGaAsP (approximately 0.95eV) layer and an InGaAsP (approximately 1.13eV) layer having a combined thickness of approximately 125Å to 155Å. It should be noted, that in an alternative embodiment, semiconductor structure 200 does not comprises a base-emitter graded quaternary InGaAsP layer forming an abrupt junction.

Overlying a first portion of the base-emitter graded quaternary InGaAsP layer 260 is an emitter layer 270. Emitter layer 270 comprises InP n-doped with a concentration in the range of approximately  $1 \times 10^{17} \text{ cm}^{-3}$  to  $1 \times 10^{18} \text{ cm}^{-3}$ . Emitter layer 270 comprises InP layer having a thickness in the range of approximately 400Å to 800Å, which is n- doped with a concentration in the range of approximately  $2 \times 10^{17} \text{ cm}^{-3}$  to  $1 \times 10^{18} \text{ cm}^{-3}$ .

Emitter layer 270 supports an emitter contact layer 280. Emitter contact layer 280 comprises n+ type doped InGaAs having a dopant concentration of approximate  $2 \times 10^{19} \text{ cm}^{-3}$  to  $1 \times 10^{20} \text{ cm}^{-3}$ . Emitter contact layer 280 also comprises a thickness in the range of approximately 500Å to 2500Å. In alternative

embodiment, emitter contact layer **280** comprises n+ type doped InAs having a dopant concentration of approximate  $2 \times 10^{19} \text{ cm}^{-3}$  to  $1 \times 10^{20} \text{ cm}^{-3}$  and a thickness in the range of approximately 200Å to 500Å.

5           An emitter contact pad **290** is also formed overlying emitter contact layer **280**. Emitter contact pad **290** comprises a Pt layer, having a thickness in the range of approximately 360Å to 440Å, overlying an Au layer, having a thickness in the range of approximately 1000Å to 10,000Å, overlying a Pt layer, having a thickness in the range of approximately 315Å to 385Å, overlying a Pd layer  
10           having a thickness in the range of approximately 45Å to 55Å. Pad **290** serves as a self-aligning etch mask in the formation of a base contact pad(s) **300**. Prior to undergoing the process of the present invention, an over-etch step is performed on structure **200** to obtain an undercut of at least 500Å underneath on pad **290**. Contact pad **290** thereafter serves as the etch mask for the emitter layer **280**  
15           which in turn has an undercut of at least 500Å created after an over etch step.

Moreover, at least one base contact pad **300** is formed overlying a portion of emitter-base graded quaternary layer **260**. At least one collector contact pad **310**, similarly, overlies subcollector layer **220**. Base and collector contact pads  
20           **300** and **310** comprise a combination of Pd, Pt, and Au. Base contact pad(s) **300** comprises an Au layer having a thickness in the range of approximately 540Å to 660Å overlying a layer of Pt having a thickness in the range of approximately 360Å to 440Å, overlying a Pd layer having a thickness in the range of approximately 35Å to 50Å. Likewise, collector contact pad(s) **310** comprises a  
25           layer of Au having a thickness in the range of approximately 5400Å to 6600Å, overlying a layer of Pt having a thickness in the range of approximately 315Å to 385Å, overlying a layer of Pd having a thickness in the range of approximately 45Å to 55Å. It is advantageous for the collector pad(s) **310** to reach the height of base pad(s) **300**, within +/- 10 percent of each other, as depicted by the dotted

lines in FIG. 4. To ensure the relative proper heights of the pads, the profile of the structure 200 may be checked with a DEKTAK stylus profilometry tool.

Referring to FIG. 5, a cross-sectional view of a process step according to the present invention is illustrated. To provide sufficient electrical access to the double heterojunction bipolar transistor, at least one collector post 320 and at least one base post 330 are formed overlying a portion of collector pad(s) 310 and a portion of base pad(s) 300, respectively. From the cross-sectional profile of structure 200 and dotted lines depicted in FIG. 5, it should be apparent to one of ordinary skill that collector and base posts 320 and 330 are intended to reach the profile height of emitter contact pad 290, within approximately +/- 10 percent (%). Similarly, one of ordinary skill should also recognize that the structure as well as its profile depicted in Figure 5 are not drawn to scale.

The fabrication sequence for the structure of FIG. 5 is as follows. Collector and base posts 320 and 330 are formed using a lift-off technique. As detailed in the above referenced U.S. Patent Number 4,214,966, the lift-off technique allows an intended space to "metallized" by delineating the space with a deposited material such as a photolithography resist. The chosen metal is then deposited by conventional methods, such as evaporation, to overly the delineated space and the deposited material. Subsequently, the photolithographic resist is then removed along with the chosen metal overlying the photolithographic resist such that delineated space is thereby defined and metallized.

In one embodiment of the present invention, collector and base posts 320 and 330 comprise a combination of Ti, Au and Pt. With these selected metals, it should be apparent to one of ordinary skill that the lift-off technique may be repeated to form collector and base posts 320 and 330.

In a further embodiment, collector and base posts 320 and 330 comprise a layer of Au having a thickness in the range of approximately of 5400Å to 6600Å, overlying a layer of Pt having a thickness in the range of approximately of 315Å to 385Å, overlying a layer of Ti having a thickness in the range of approximately of 45Å to 55Å. By selecting these dimensional criteria, collector and base posts 320 and 330 approximately reach the height of emitter contact pad 290 within a range of approximately 900Å to 1000Å.

Referring to FIG. 6, a cross-sectional view of the result of a second step of the present invention is illustrated. By forming collector and base posts 320 and 330, a resultant profile is created for the desired semiconductor device. A passivation layer 340 is then formed encapsulating the resultant semiconductor device to electrically isolate the device from the external environment and prevent damage and interference to the device elements. Passivation layer 340 is applied by spinning a suitable material onto the surface to produce a layer of polymer encapsulant. It is advantageous to use a polymer layer comprising benzocyclobutene ("BCB") created from the polymerization of Cyclotene™ made available by Dow Chemical for passivation layer 340. Alternate materials will be apparent to one of ordinary skill in the art, including Accuglass™ spin on glass made available by Allied Signal Inc. The BCB is spun on within a range 2000 to 5,000 revolutions per minute (rpm) for a period(s) ranging from 20 to 200 seconds. It is beneficial, in the present case, to spin on the BCB at 2000 RPM for 60 seconds, to reach a height of at least approximately twice the device structure, or within a range of at least approximate 1800 μm to 2200 μm.

Subsequently, structure 200 comprising passivation layer 340 is cured by a heating step. The curing step may be realized at a temperature of 300°C in an atmosphere of N<sub>2</sub> for approximately 10 minutes. Heating times and temperatures can vary substantially and still yield acceptable results, though,

and, as such, an approximate temperature range of 250 to 350°C, and a time having an approximate range of 1 to 30 minutes are operable conditions. It should be noted that alternate atmospheres during the heating step may also be employed, but advantageously should not include O<sub>2</sub> at greater than 200 parts per million. The heating technique used in the processes described here was a conventional hot plate anneal step. However, other heating techniques may also be considered including, for example, Rapid Thermal Annealing ("RTA"), as well as the utilization of an oven or furnace.

In one embodiment of the present invention, the curing step comprises three individual sub-steps. Initially, a flush heating step is performed on structure 200 in an atmosphere of N<sub>2</sub> at a temperature range of approximately 45°C to 55°C for approximately 30 minutes. Subsequently, a heating step in an atmosphere of N<sub>2</sub> at a temperature range of approximately 140°C to 160°C for approximately 60 minutes is executed. A second heating step is performed thereafter in an atmosphere of N<sub>2</sub> at a temperature range of approximately 250°C to 350°C for approximately 1-40 minutes.

During the curing process of the passivation layer, the metal pads and posts are annealed, generally. More specifically, base contact pad(s) 300 diffuses into and through (not shown) emitter-base graded quaternary layer 260 to make ohmic contact with base layer 250. Once encapsulated and heated, a planarization step is in effect completed on the heated encapsulated structure.

In one embodiment of the present invention, the passivation layer 340 is planarized as a result of executing two of the hereinabove steps. Upon performing the spinning step to form the passivation layer, the surface is planarized. In further embodiment of the present invention, passivation layer 340 is forty five percent (45%) to fifty five percent (55%) planarized by this

spinning step, while the remaining amount of planarization is achieved by performing the hereinabove curing step. In yet a another embodiment of the present invention, this remaining amount of passivation layer 340 to be planarized is the result of executing the hereinabove heating step in an atmosphere of N<sub>2</sub> at a temperature range of approximately 140°C to 160°C

Referring to **FIG. 7**, a cross-sectional view of a subsequent step of the present invention is illustrated. Here, a series of external contacts are formed. This step is realized by removing unwanted segments from layer 340 on the planarized, cured and encapsulated structure of **FIG. 6**. Using an etching step, portions of emitter contact pad 290, collector post 320 and base post 330 are exposed through layer 340.

In one embodiment of the present invention, a dry etch is employed for the etching step. The dry etch step is advantageously realized by a Reactive Ion Etch ("RIE") using a Plasma Therm SLR 770 system at a bias of 100V dc, and a pressure of approximately 15mTorr. In an alternative embodiment, an Inductively Coupled Plasma ("ICP") or Electro Cyclotron Resonance ("ECR") etch step may also be used. It is advantageous to use CF<sub>4</sub>:O<sub>2</sub> at a ratio of 40:60 for this dry etch step. However, other fluorine -oxygen based etchants may be used, such as SF<sub>6</sub>:O<sub>2</sub> at a ratio of 6:10, to obtain an etch rate of approximately 500 Å/minute. By this etch step, approximately 1000Å to 5000Å of passivation layer 340 are removed to ensure that posts 320 and 330 are exposed. Moreover, any residue from passivation layer 340 is removed as well. Thus, the base, emitter and collector are made accessible through the planarized, cured and encapsulated structure to enable subsequent interconnects for the completed III-V semiconductor device.

In still, yet another alternate embodiment of the present invention, an endpoint detection scheme is employed. Here, endpoint detection controls the etching of the planarized heated passivation layer 340. In this step, Optical Emission Spectroscopy ("OES") may be employed using an ISA SOFIE DIGISEM

5 550.

Referring to FIG. 8, a top down view of the completed III-V semiconductor device as depicted in FIG. 7 is illustrated. From this vantage point, emitter contact pad 290, as well as collector and base posts 320, 330 are shown isolated by passivation layer 340. In one embodiment of the present invention, collector and base posts 320, 330 each have dimensions of  $1.4 \times 1.4 \mu\text{m}$ , emitter contact pad 290 is dimensionally  $1.2 \times 3 \mu\text{m}$  and spaced from base post 320 by  $0.8 \mu\text{m}$ , while collector contact pad 310 is spaced  $0.8 \mu\text{m}$  from emitter-base quaternary graded layer 260.

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Referring to FIG. 9, a graph of Frequency (GHz) versus  $I_C$  Current (A) characteristics is illustrated. Here, the radio frequency ("RF") performance of the hereinabove fabricated III-V semiconductor device is compared with a similar III-V semiconductor device having a larger emitter mesa size. As shown in FIG. 9, with the emitter size scaled down in size, a device cut-off frequency ( $f_T$ ) remained substantially constant in the range of approximately 160 to 170 GHz. This is primarily attributable to the fact that  $f_T$  is primarily determined by the base-collector transit time. However, because of the reduced parasitics in the device created by closely spaced contacts and reduced base mesa area of the instant invention, the maximum frequency ( $f_{\text{MAX}}$ ) of the device substantially increased from approximately 155GHz to 200GHz. It should be noted that the device parasitics, such as the base-collector capacitance, were reduced by the instant invention from approximately 25fF to 12fF.

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While the particular invention has been described with reference to illustrative embodiments, this description is not meant to be construed in a limiting sense. It is understood that although the present invention has been described, various modifications of the illustrative embodiments, as well as additional embodiments of the invention, will be apparent to one of ordinary skill in the art upon reference to this description without departing from the spirit of the invention, as recited in the claims appended hereto. Thus, while detailed the present invention details a process of fabricating a DHBT, it should be apparent to one of ordinary skill that the present invention may be applied to HBTs, as well as other semiconductor devices in need of the advantages and benefits of the present invention. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.

**What is Claimed is:**

1. A method of fabricating a bipolar semiconductor device from a structure,  
the structure comprising:

a substrate;

a semiconductor subcollector layer overlying the substrate;

a semiconductor collector layer overlying the semiconductor subcollector  
contact layer;

a semiconductor graded base-collector layer overlying the semiconductor  
collector layer;

a semiconductor base layer overlying the semiconductor graded base-  
collector layer;

a semiconductor graded emitter-base layer overlying the semiconductor  
base layer;

a semiconductor emitter overlying a first portion of the semiconductor  
graded emitter-base layer;

at least one base contact pad overlying a second portion of the  
semiconductor graded emitter-base layer;

an emitter contact pad overlying the semiconductor emitter having a  
height; and

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at least one collector contact pad overlying at least one of the semiconductor sub collector layer and the semiconductor collector layer, wherein the method comprises the steps of:

forming at least one collector contact post and at least one base contact post, the at least one collector contact post overlying the at least one collector contact pad and the at least base contact post overlying the at least one base contact pad, the at least one collector contact post and the at least one base contact post substantially reaching the emitter contact pad height;

forming a passivation layer to encapsulate the structure, the at least one collector contact post, and the at least one base contact post;

curing the passivation layer; and

exposing the at least one collector contact post, the at least one base contact post, and the emitter contact pad through the cured passivation layer to form the bipolar semiconductor device.

- 1 2. A method of claim 1, further comprising the step of substantially
- 2 planarizing the passivation layer, the step of substantially planarizing the
- 3 passivation layer comprising the steps of the forming a passivation layer and the
- 4 curing of the passivation layer.

1 3. The method of claim 1, wherein the step of forming at least one collector  
2 contact post and at least one base contact post comprises a lift-off step.

1 4. The method of claim 1, wherein at least one of the at least one collector  
2 contact post and the at least one base contact post comprises Pt, Au and Ti.

1 5. The method of claim 1, wherein the step of forming a passivation layer  
2 comprises spinning on benzocyclobutene ("BCB").

1 6. The method of claim 1, wherein the step of curing the passivation layer  
2 comprises the step of heating the passivation layer in an N<sub>2</sub> atmosphere to a  
3 temperature substantially in the range of 250-350°C for a period substantially in  
4 the range of 1-30 minutes.

1 7. The method of claim 1, wherein the step of exposing the at least one  
2 collector contact post, the at least one base contact post, and the emitter contact  
3 pad through the cured passivation layer comprises the step of etching the cured  
4 passivation layer.

1 8. The method of claim 7, wherein the step of etching the cured passivation  
2 layer further comprises the step of detecting an endpoint to the etching of the  
3 planarized cured passivation layer.

1 9. The method of claim 7, wherein the step of etching the cured passivation  
2 layer comprises a Reactive Ion Etching step.

1 10. The method of claim 7, wherein the step of etching employs a chemistry of  
2 at least one of  $\text{CF}_4:\text{O}_2$  at an approximate ratio of 40:60 and  $\text{SF}_6:\text{O}_2$  at an  
3 approximate ratio of 6:10.

1 11. A method of fabricating a III-V heterojunction bipolar semiconductor  
2 device from a structure, the structure having a height and comprising:

3  
4 an InP substrate;

5  
6 an n+ InGaAs subcollector overlying the substrate;

7  
8 an n- InP collector overlying the subcollector;

9  
10 a first graded quaternary InGaAsP base-collector layer overlying the  
11 collector;

12  
13 an InGaAs base overlying the first graded quaternary layer;

14  
15 a second graded quaternary InGaAsP emitter-base layer overlying the  
16 base;

17  
18 an n- InP emitter overlying a first portion of the second graded quaternary  
19 layer;  
20

at least one base contact pad overlying a second portion of the second graded quaternary layer, the base contact comprising at least one of Pd, Pt and Au and having a base contact pad height;

an n+ InGaAs emitter contact pad overlying the emitter and having an emitter contact pad height; and

at least one collector contact pad overlying at least one of the subcollector and the collector, the at least one collector contact pad substantially reaching the base contact pad height, wherein the method comprises the steps of:

forming at least one collector contact post overlying the at least one collector contact pad and at least one base contact post overlying the at least one base contact pad, the at least one collector contact post and the at least one base contact post substantially reaching the emitter contact pad height and comprising at least one of Ti, Pt and Au;

encapsulating the structure, the at least one collector post, the at least one base post and the emitter contact pad with a polymer layer having a encapsulating height of approximately twice the height of the structure;

curing the polymer layer in an N<sub>2</sub> atmosphere substantially in the range of 250-350°C for a time period substantially in the range of 1-30 minutes to anneal the pads, the posts, and allow the base contact pad to directly interface with the base; and

50 etching the cured polymer layer to expose the at least one base  
51 post, the at least one collector post and the emitter contact pad  
52 through the cured polymer layer and form the III-V heterojunction  
53 bipolar semiconductor device.

1 12. The method of claim 11, wherein the step of forming a collector contact  
2 post and a base contact post comprises a lift-off step.

1 13. The method of claim 11, wherein the polymer layer is substantially  
2 planarized by the step of encapsulating with a polymer layer step and the step of  
3 curing the polymer layer step.

1 14. The method of claim 11, wherein the polymer layer comprises spun on  
2 benzocyclobutene.

1 15. The method of claim 11, wherein the step of etching the cured polymer  
2 layer comprises a Reactive Ion Etching step and employs at least one of  $\text{CF}_4$  at an  
3 approximate ratio of 40:60 and  $\text{SF}_6:\text{O}_2$  at an approximate ratio of 6:10.

1 16. A method of fabricating a semiconductor device having a semiconductor  
2 region, the method comprising the steps of:  
3  
4 forming at least one conductive post overlying the semiconductor region  
5 to form a structure;

6  
7 encapsulating the structure and the at least one conductive post to form a  
8 planarized cured passivation layer; and

9  
10 exposing the at least one conductive post through the planarized cured  
11 passivation layer to form the semiconductor device.

1 17. The method of claim 16, wherein the step of forming at least one  
2 conductive post comprises a lift-off step, and the at least one conductive post  
3 comprises at least one of Pt, Au and Ti.

1 18. The method of claim 16, wherein the step of encapsulating the structure  
2 and the at least one conductive post comprises the steps of:

3  
4 forming the passivation layer by spinning on benzocyclobutene ("BCB");  
5 and

6  
7 heating the passivation layer in an N<sub>2</sub> atmosphere to a temperature  
8 substantially in the range of 250-350°C for a period substantially in the  
9 range of 1-30 minutes, such that the passivation layer is spun on, cured  
10 and planarized.

1 19. The method of claim 16, wherein the step of exposing the at least one  
2 conductive post comprises the step of etching the planarized cured passivation  
3 layer.



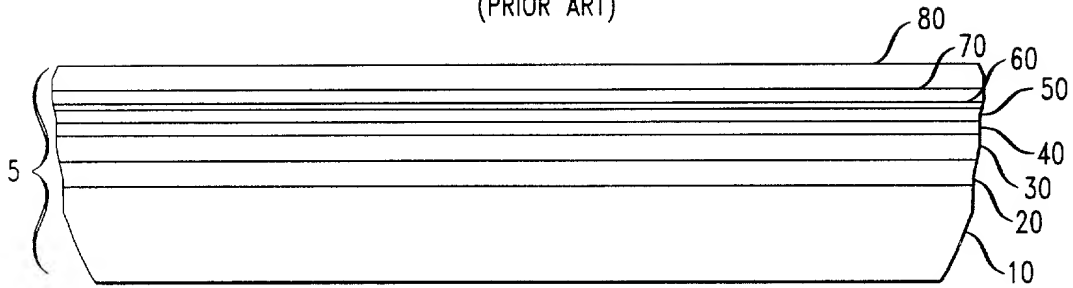
- 1 20. The method of claim 19, wherein the step of etching the planarized cured
- 2 passivation layer comprises a Reactive Ion Etching step and employs a chemistry
- 3 of at least one of  $\text{CF}_4:\text{O}_2$  at an approximate ratio of 40:60 and  $\text{SF}_6:\text{O}_2$  at an
- 4 approximate ratio of 6:10.

### ABSTRACT

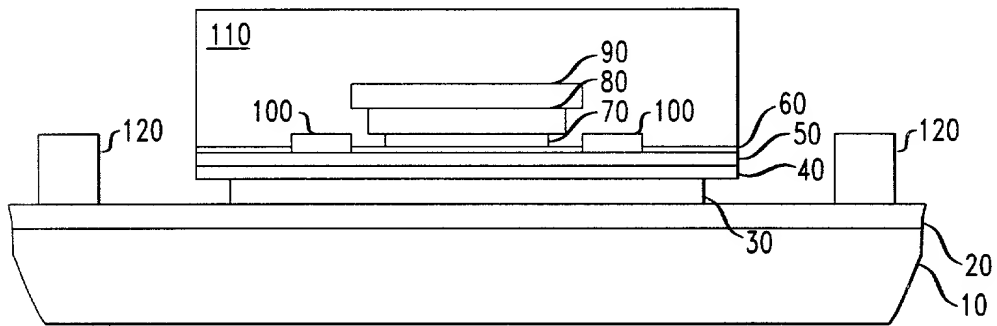
5 A method of fabricating a III-V heterostructure semiconductor device. The method includes the steps of forming at least one conductive post overlying a semiconductor region to form a structure, encapsulating the structure and the conductive post to form a planarized cured passivation layer, and exposing the conductive post through the planarized cured passivation layer to form the semiconductor device.

1/3

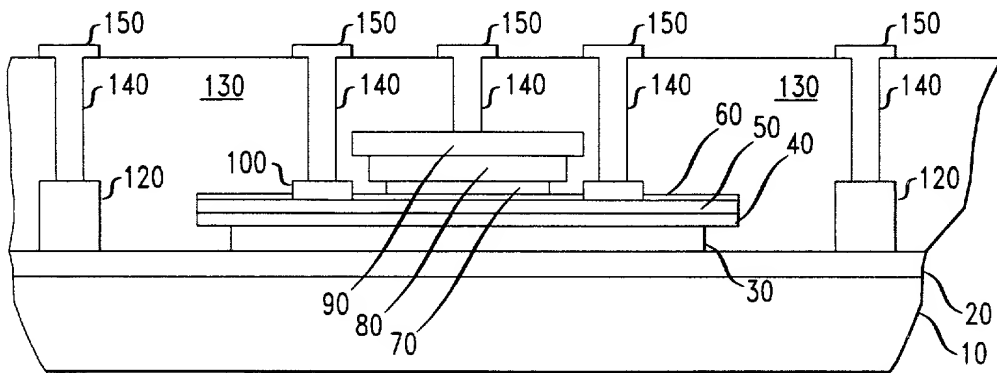
*FIG. 1*  
(PRIOR ART)



*FIG. 2*  
(PRIOR ART)



*FIG. 3*  
(PRIOR ART)



2/3  
FIG. 4

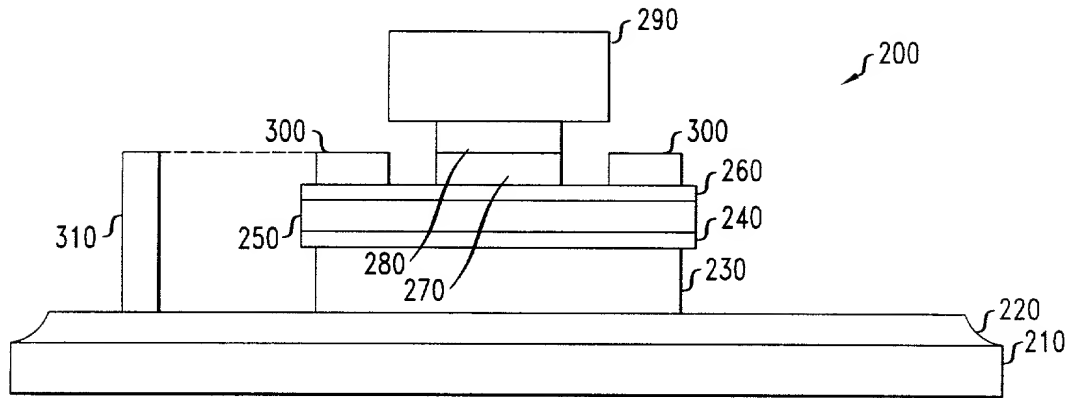


FIG. 5

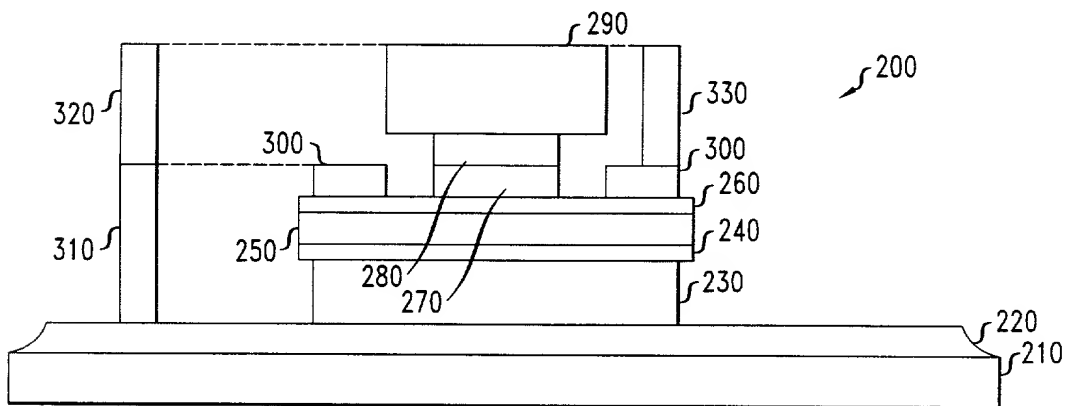
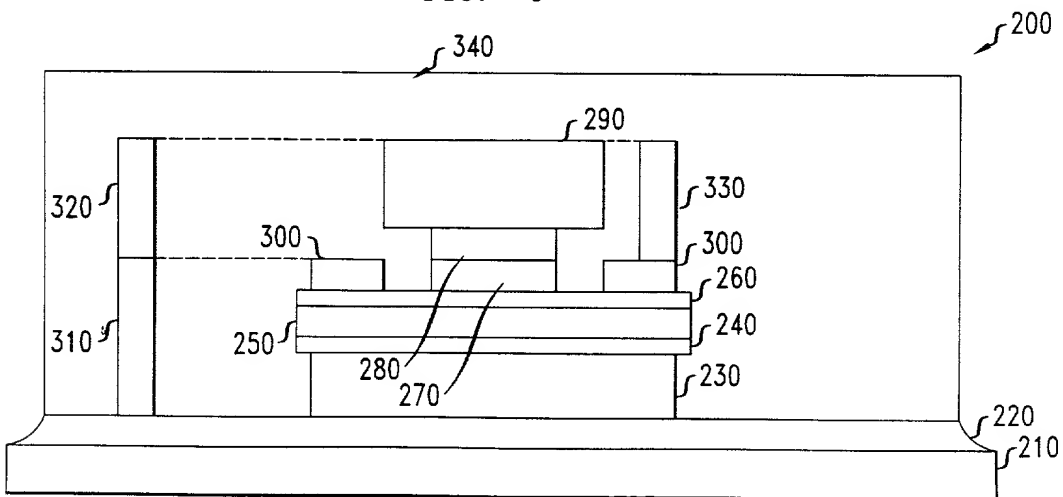


FIG. 6



3/3  
FIG. 7

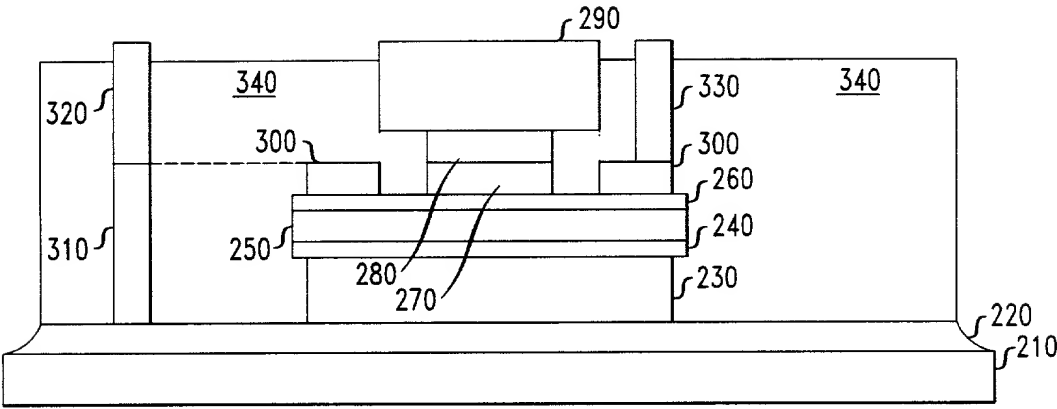


FIG. 8

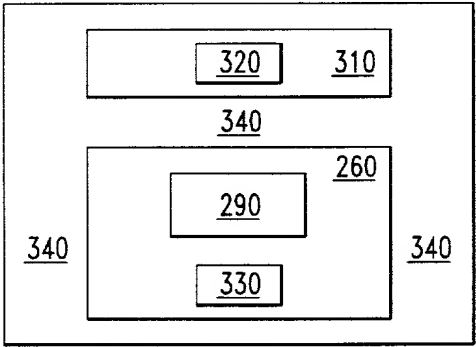
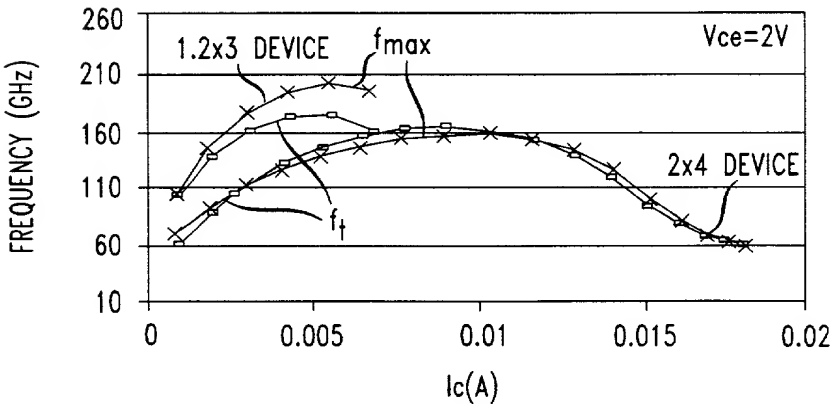


FIG. 9



IN THE UNITED STATES  
PATENT AND TRADEMARK OFFICE

Declaration and Power of Attorney

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled **A Method Of Fabricating A Heterjunction Bipolar Transistor** the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

None

I hereby claim the benefit under Title 35, United States Code, 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

None

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorney(s) with full power of substitution and revocation, to prosecute said application, to make alterations and amendments therein, to receive the patent, and to transact all business in the Patent and Trademark Office connected therewith:

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